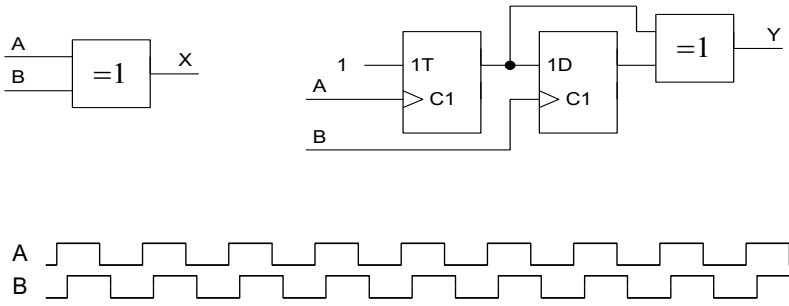
ELEC50001 EE2 Circuits and Systems

Problem Sheet 4

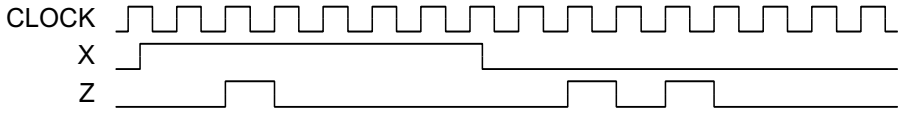
(Counters and Shift Registers – *Lecture 9)*
(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1B. Q2:0 is the output of a 3-bit binary counter whose input is a constant frequency squarewave, CLOCK. Give a Boolean expression for Z in terms of Q2:0 such that Z is high whenever Q2:0 has the value 6. Draw a timing diagram showing the waveforms of CLOCK and Z and the value of Q2:0 during each clock cycle. Indicate on your diagram where glitches might occur in Z.

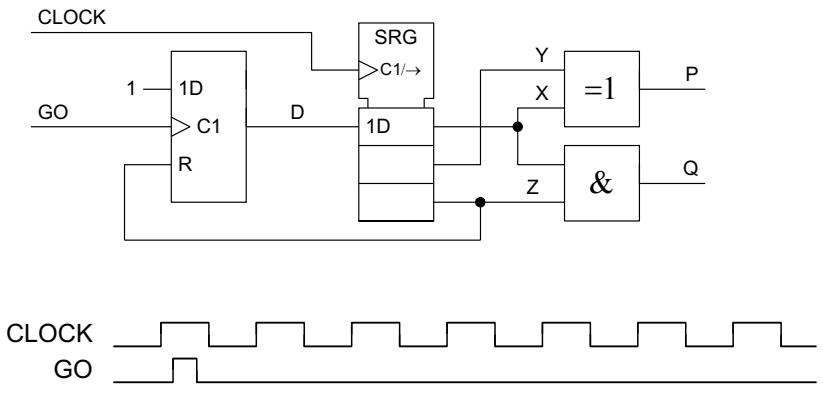
2C. The diagram shows two *phase-detector* circuits. Inputs A and B are symmetrical squarewaves with the same frequency but differing phases. Complete the timing diagram by showing the waveforms of X and Y for the case when B lags A by 45°. If logical 0 and 1 correspond to 0 V and 5 V respectively, sketch graphs showing how the DC components (i.e. average values) of X and Y vary with the phase difference.



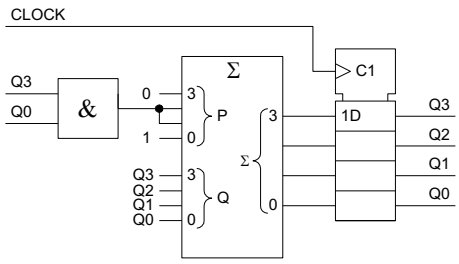
3B. The signal X forms the input to a shift register that is clocked by CLOCK↑. As shown in the timing diagram, the signal Z gives one pulse when X goes high and two pulses when it returns low. If the successive outputs from the shift register are A, B, C, … derive a Boolean expression for Z.



4B. Complete the timing diagram by drawing the waveform of P and Q. Explain why only one of these signals is certain to be glitch-free. If the GO pulse occurs at a random time with respect to the CLOCK, determine the average time delay in CLOCK periods between the GO↑ edge and the Q↑ edge. Implement this circuit in Verilog.



5C. The diagram shows an AND gate, a 4-bit register and an adder connected together to form a counter. List the values taken by the P input of the adder for all possible values of Q3:0. Draw a state diagram showing the sequence of values taken by Q3:0 on successive CLOCK pulses.



6C. Modify the above circuit so that it follows the count sequence 1, 2, 3, …, 9, 10, 1, 2, 3, …. Draw a state diagram for your revised circuit. Implement this circuit in Verilog.

7B. In lecture 5 slide 17, a 4-bit linear feedback shift register (LFSR) is implemented with the primitive polynomial $1 + X^3 + X^4$. An alternative primitive polynomial that also gives a maximal cycle length of 15 with a 4-bit LFSR is: $1 + X + X^4$ as shown in the notes for that slide. Derive the sequence resulted in this alternative polynomial. Implement this in Verilog.

8B. Design a maximal length 7-bit LFSR in Verilog.

9C. The DE10-Lite board has a 50MHz system clock available. Design a clock divider circuit that produces a 20 ns pulse every 1 microsecond in schematic form and in Verilog form.